

Amendments to the Specification:

Please replace paragraph [0003] with the following amended paragraph:

[0003] This application is a continuation of U.S. Patent Application Serial No. 09/767,086, filed January 22, 2001, which issued as U.S. Patent No. 6,715,089 on March 30, 2004, and is incorporated by reference as if fully set forth.

Please replace paragraph [0023] with the following amended paragraph:

[0023] Figure 2 illustrates a computer system having separate monitoring mechanisms for a microprocessor 90 and a graphics processor 115 which process instructions queued in an instruction cache 120 and/or a memory buffer 125. The microprocessor 90 and the graphics processor 115 118 each have their own load and clock estimation device 100, 105, respectively. ~~Each estimation device 100, 105 controls the clocking frequency of its processor 90, 115~~ The first load and clock estimation device 100 controls the frequency of a clocking signal outputted from a first clock 95 to the microprocessor 90. The second load and clock estimation device 105 controls the frequency of a clocking signal outputted from a second clock 110 to the graphics processor 115.

Please replace paragraph [0028] with the following amended paragraph:

[0028] To enhance performance, a short term and a long term estimate may be used, as shown in Figure 4. ~~Built onto the An integrated circuit (IC) microprocessor chip 160 includes is a short term instruction queue monitoring and data collection device 165, a short term estimation load estimation blocks device 165, 170, an optimum clock estimation device 175, a clock 180 and a microprocessor 185.~~ The short term ~~blocks 165, 170 analyze~~ load estimation device 170 analyzes a set of instructions 190 stored in a cache (not shown) on the IC chip 160. Since the analysis is performed on a silicon level, the analysis is performed frequently.

Please replace paragraph [0029] with the following amended paragraph:

[0029] Long term load estimation devices blocks 205, 210 analyze a set of instructions 195 queued off-chip, such as in an off-chip cache or in memory. Based on the long term analysis, a the long term optimum clock estimation block device 175 on the IC chip 160 determines a preferred long term clocking frequency for the clock 180. The update of the long term frequency may be performed at the same or a lower rate than the short term analysis. ~~On chip, an~~ The optimum clock estimation device 175 also block determines the clock frequency for the clock 180 based on the short term analysis and the preferred long term clocking frequency. Using this two-tier approach, short term performance can be adjusted at a fast rate.